Claims

We claim:

1. A method for manufacturing a ferroelectric capacitor comprising the steps of:

forming a substructure of the capacitor having a contact plug passing therethrough for electrically connecting a bottom electrode of the capacitor to an underlying active layer;

depositing over the substructure the bottom electrode including a barrier layer intermediate therebetween;

depositing over the bottom electrode a ferroelectric layer such that the diffusion of contaminants from the ferroelectric layer to the contact plug is inhibited by the intermediate barrier layer;

depositing over the ferroelectric layer a top electrode;

depositing over the top electrode, the underlying ferroelectric layer and the bottom electrode a first hardmask;

etching to pattern the top electrode using the first hardmask;

depositing over the remaining portions of the first hardmask and on the bottom electrode an additional hardmask;

etching to pattern the bottom electrode using a first recipe resulting in the formation of a first fence clinging to sidewalls of the additional hardmask, bottom electrode and barrier layer; and

etching the intermediate barrier layer using a second recipe resulting in the formation of a second fence clinging to and structurally supported by the first fence while at the same time etching away a substantial portion of the first

fenc to remove the structural support provided to the second fence so that the second fence is lifted-off from the sidewalls leaving the sidewalls substantially free of clinging fences.

2. The method of Claim 1 wherein the intermediate barrier layer has a composition including Iridium.

3. The method of Claim 2, wherein 30% to 90% of the barrier layer not protected by the additional hardmask is removed during the etching using the first recipe.

4. The method of Claim 1, wherein the etching of the intermediate barrier layer using the second recipe continues until portions of the substructure are also etched.

5. The method of Claim 1, wherein the additional hardmask is tapered at an angle steeper than 60 degrees.

6. The method of Claim 1, wherein the contaminants include oxygen.

7. The method of Claim 1, wherein the first recipe is a fluorine-based recipe.

8. The method of Claim 1, wherein the second recipe is a CO-based recipe.

9. The method of Claim 1, wherein the additional hardmask is formed from TEOS.

10. A ferroelectric capacitor comprising:

a ferroelectric layer between a top and a bottom electrode;

a contact plug passing through a substructure of the ferroelectric capacitor and electrically connecting the bottom electrode to an active layer;

a barrier layer separating the bottom electrode from the substructure and contact plug for inhibiting the diffusion of oxygen from the ferroelectric layer to the contact plug, the barrier layer having sidewalls changing from a relatively low taper angle above a sidewall transition to a relatively steep taper angle below the sidewall transition;

a first hardmask covering the top electrode for protecting portions of the top electrode during a first etching step for patterning the top electrode; and

an additional hardmask deposited over remaining portions of the first hardmask and on the bottom electrode for protecting portions of the bottom electrode during a second etching step.

11. The ferroelectric capacitor of Claim 10, wherein:

the relatively low taper angle of the sidewalls of the barrier layer above the sidewall transition is formed during the first etch using a fluorine-based etching recipe; and

the relatively steep taper angle of the sidewalls of the barrier layer below the sidewall transition is formed during a second etch using a CO-based etching recipe.

12. The method of Claim 10, wherein the additional hardmask is tapered at an angle steeper than 60 degrees.

13. An FeRAM cell using the ferroelectric capacitor of Claim 10 for storing data.

14. A device comprising:

a barrier layer for blocking the diffusion of contaminants from an intermediate layer; wherein

the barrier layer has sidewalls changing from a relatively low taper angle above a sidewall transition to a relatively steep taper angle below the sidewall transition;

the relatively low taper angle of the sidewalls of the barrier layer above the sidewall transition is formed during the first etch using a fluorine-based etching recipe; and

the relatively steep taper angle of the sidewalls of the barrier layer below the sidewall transition is formed during a second etch using a CO-based etching recipe.